REMARKS

The Office action dated May 27, 2008 has been received and its contents carefully noted. Claims 24-46 are pending in this application. In the Office action, all pending claims are rejected. With this paper, claims 24, 41-42 and 45 are amended, none are canceled, and claims 47-58 are added, so that claims 24-58 remain in the application.

Applicant's attorney, Alfred A. Fressola, would like to thank Examiner Campos for her helpful comments made during a telephone interview on August 25, 2008. At that time, Examiner Campos stated that her interpretation of MPEP 2106 II (c) is that the phrase "configured to" means an intended use that does not require the recited functionality. This interpretation was specifically discussed with respect to the objected phrase referenced at section 28 of the Official Action. In response thereto, applicant has deleted the word "for" from the referenced claims, which according to Examiner Campos would overcome the objection.

New claims 47-57 ultimately depend from independent method claim 41 and find support in corresponding dependent claims 25-33 and 35-36, which depend from independent device claim 24. New claim 58 is an apparatus claim that finds support in corresponding independent device claim 24. No new matter has been introduced.

As noted above, applicant has amended independent claims 24, 42 and 45 to remove the phrase "for" in order to eliminate any interpretation of the limitation as intended use, as indicated by the Office in section 28 of the Response to Arguments section of the Office action. As amended, it is clear that there are "at least two access controllers selectively providing" a function, not access controllers intended to perform the recited function. No new matter has been introduced by way of amendment.

Applicant has also amended independent claims 24, 41-42 and 45 to replace the phrase "or individual addressing" with "and individual addressing" in order to respond to the Office's assertion at section 29 of the Response to Arguments section of the Office action, which indicates that there is no requirement for the prior art of record to teach sole addressing in order for the prior art of record to read on the claimed invention because the prior art of record teaches individual addressing. Applicant has removed the alternative phrase "or" to indicate that the claimed invention requires the ability to carry out both sole and individual addressing, thus applicant respectfully asserts that the prior art of record

must also teach sole addressing as claimed in order to read on the claimed invention. No new matter has been introduced by way of amendment. This amendment was also discussed by applicant's attorney with Examiner Campos on August 25, 2008.

35 U.S.C. 103(a) Rejections

At sections 3-23 of the Office action, the Office rejects claims 24-46 under 35 U.S.C. 103(a) as being unpatentable over *Camacho et al.* (U.S. 6,167,487, hereafter referred to as *Camacho*) in view of *Ware et al.* (U.S. 6,826,657, hereafter referred to as *Ware*). Of these claims, claims 24, 41-42 and 45 are independent. At sections 24-31 of the Office action, the Office presents arguments concerning the prior art rejections. For the reasons set forth below, the applicant respectfully requests reconsideration of the rejection.

In the Office action, the Office correctly asserts that the *Camacho* reference does not disclose expressively the case of sole addressing in which the data is provided through data ports of both terminals. However, the Office is of the opinion that *Ware* discloses this feature. In particular, the Office relies on col. 15, l. 47- col. 16, l. 3, as well as col. 32, l. 16-23, col. 7, l. 6-25.

It is applicant's opinion that the feature of sole addressing and accessing the data, where "access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within all of the two memory areas through data ports of both terminals" is not disclosed by Ware.

To define applicant's position, Figure 6a of Ware with additional reference signs QDx, QDy and lines is depicted hereinafter.

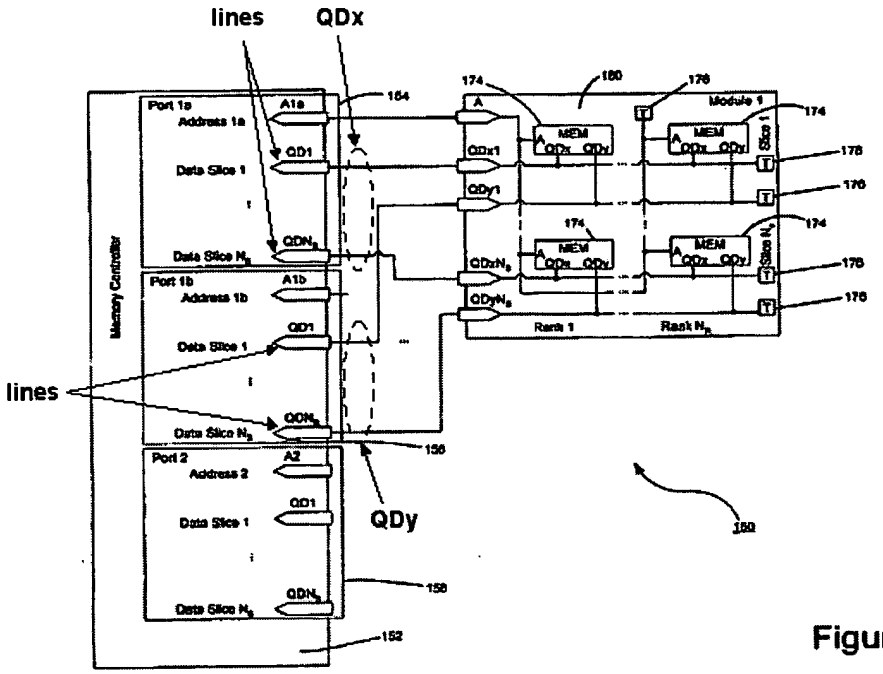


Figure 6A

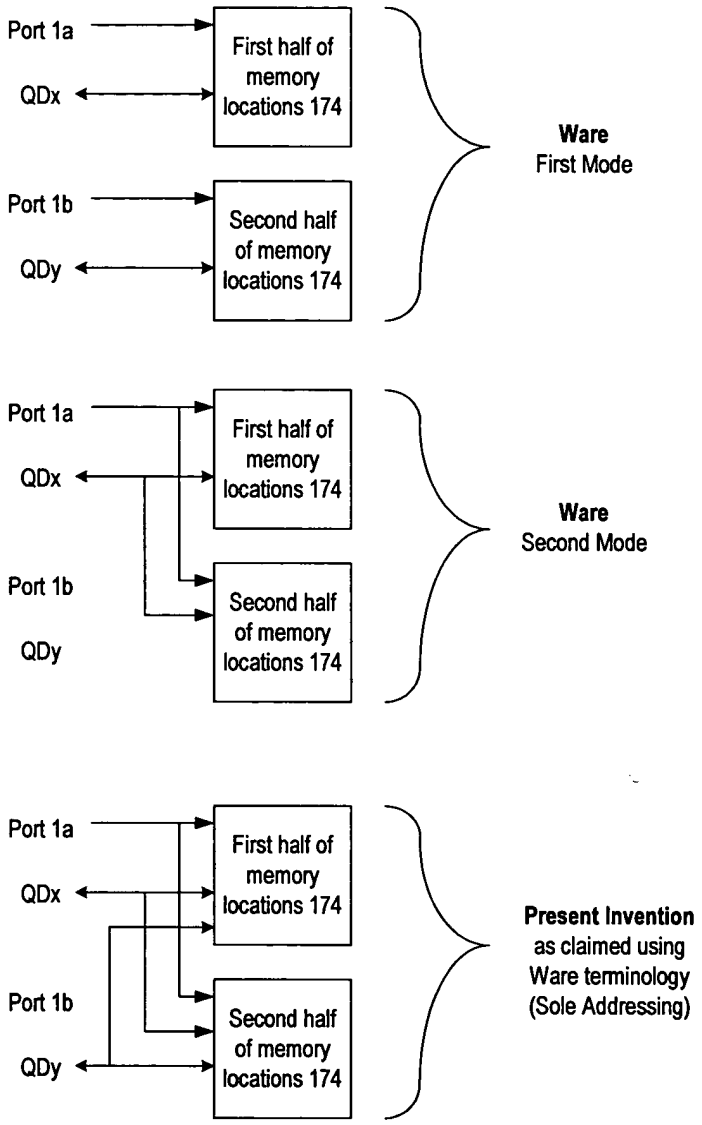
As can be seen from Figure 6A of Ware, a first port 1a and a second port 1b are provided which correspond to the first terminals and second terminals according to the present invention. Furthermore, each of these ports 1a and 1b is connected to memory components 174 of a memory 160. Ware discloses explicitly that "*each memory component (MEM) has <u>two</u> data bus ports denoted QDx and QDy*" (Ware: col. 15, l. 13-14). In other words, according to Ware, only two data busses are provided for connecting ports 1a and 1b to the memory components 174, wherein a data bus corresponds to the data ports of the first or second terminals according to the present invention. More particularly, Ware teaches explicitly that QDx or QDy denotes each merely <u>one data bus</u> (Ware: col. 15, l. 22-23: "*...QDx data bus, and the QDy data bus...*"). In support, both data buses are denoted by QDx or QDy in Figure 6A. In general, a bus, in particular a parallel bus, comprises several parallel lines, ports or pins. According to Ware, each data bus QDx or QDy comprises N_S lines, ports or pins. By way of example, if the number of lines is 16, it may be possible to process 16 bits in parallel. However, it is still only <u>one</u> bus having 16 parallel lines or ports. In Figure 6A, only the first line QD1 and the last line QDN_S of the data bus QDx and QDy respectively are depicted while the further lines are indicated by

dots. Hence, the two data busses QDx and QDy are the only data busses having N_S lines according to Ware.

Furthermore, the data bus QDx is configured to only connect port 1a to the memory components 174 while data bus QDy is configured to only connect port 1b to the memory components 174 (Ware: col. 15, l. 13-23; Fig. 6a, 6b). In addition, Ware discloses that access to the memory module 160 may be done in a first mode. Within the first mode, half of the storage locations in the memory components 174 are accessible through the QDx data bus and the other half of the storage locations in the memory components 174 is accessible through the QDy data bus (Ware: col. 15, l. 20-23, Fig. 6a). Thus, in the first mode, one data bus provides access to half of the memory locations in the memory components 174 and the other data bus provides access to the other half of the memory locations in the memory components 174.

Further, there is a second mode according to Ware, within which all of the storage locations of the memory components 174 are accessible through the QDx data bus, while the QDy data bus is unused (Ware: col. 15, l. 20-23).

Such a technique as disclosed by Ware is unlike the present invention as claimed. In short, Ware provides that one data bus (QDx) can, when in the second mode, access data from all memory locations of memory components 174. Ware does not disclose or suggest that one data bus (e.g., QDx) can be combined with another data bus (e.g., QDy) to access all memory locations of memory components 174 while the addressing of the memory locations is performed solely by the address lines associated with one data bus (e.g., Port la). The attached diagram makes this distinction clear:



According to the present subject matter of claim 24, it is explicitly taught that "access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within all of the at least two memory areas through data ports of both terminals." The only busses according to Ware used by both ports 1a and 1b are data bus QDx and data bus QDy. Even if QD1 and QDN_S were understood to be two busses (which applicant does not subscribe to), and not two lines as asserted by the applicant, both QD1 and QDN_S are always and compulsorily used by the same port 1a (i.e. first terminal). It is excluded by the disclosure of Ware that QD1 or QDN_S is used by the other port 1b (i.e. second terminal). Thus, it is not possible to read the apparatus according to Ware under the present wording of claim

24. According to claim 24, two conditions must be fulfilled at the same time. The first condition is that first data ports and second data ports respectively can be used by first terminals and second terminals respectively. The second condition is that both data ports can be also used by only the first terminals or only the second terminals. These conditions are not fulfilled according to Ware, regardless of whether QD1 and QDN_S are understood to be two data busses, which applicant understands otherwise.

Indeed, Ware discloses maximizing memory bandwidth across the full memory address space (Ware: col. 32 l. 61 – col. 33, l. 6). However, compared to the present invention, the bandwidth according to Ware is limited. It is not possible to use both the data bus of the first terminal and the data bus of the second terminal at the same time by using only control and address ports of <u>one</u> of the terminals. Hence, the provided bandwidth in case of sole addressing according to Ware is half of the provided bandwidth according to the present application, since according to the present invention both data busses can be used at the same time by control and address ports of only <u>one</u> terminal. In other words, the bandwidth is significantly increased by the apparatus according to the present application.

Consequently, *Ware* does not disclose "wherein in case of sole addressing and accessing the data, the access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within all of the at least two memory areas through data ports of both terminals," as recited in claim 24. Thus, *Camacho* in view of *Ware* fails to render claim 24 obvious, and therefore applicant respectfully requests reconsideration and withdrawal of the rejection of claim 24.

Claims 41-42, 45 and 58 are independent claims which contain similar features as claim 24 described above. For at least the reasons presented above regarding claim 24, claims 41-42, 45 and 58 are also patentable over *Camacho* in view of *Ware*. Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 41-42, 45 and 58.

Claims 25-40, 43-44 and 46-57 are dependent claims and recite additional features not recited in the independent claims. For the reasons regarding independent claims 24, 41-42, 45 and 58 above, *Camacho* in view of *Ware* fails to render the claimed invention obvious. Therefore, all of the dependent claims are also patentable over the cited art.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

Dated: August 27, 2008

Cathy A. Sturmer
Agent for Applicants
Registration No. 60,869

WARE, FRESSOLA, VAN DER
SLUYS & ADOLPHSON LLP
Building Five, Bradford Green
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955